AND8408/D

Pulse Generation and Signal Conditioning Circuits Using Configurable Multifunction Logic Gates

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APPLICATION NOTE

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Introduction

A configurable multifunction logic gate is a versatile IC that can be used to create pulse generation and signal conditioning circuits. Configurable logic gates are a low cost flexible IC that can function as a buffer / inverter, AND / NAND, OR / NOR, XOR / XNOR or multiplexer. Twelve popular circuits are shown that are created by either adding an external resistor and capacitor to an input pin or by taking advantage of the inherent features of the multifunctional gates. Design examples are provided for the following circuits:

Pulse Generation Circuits

- Dual edge delay
- Leading edge delay
- Trailing edge delay
- Dual edge detector / frequency doubler
- Leading edge detector
- Trailing edge detector

Signal Conditioning Circuits

- 2−to−1 multiplexer / selector
- Voltage translator
- Power good indicator
- Switch debouncer
- Oscillators
- NRZ−to−RZ data converter

Configurable Multifunction Logic Gates

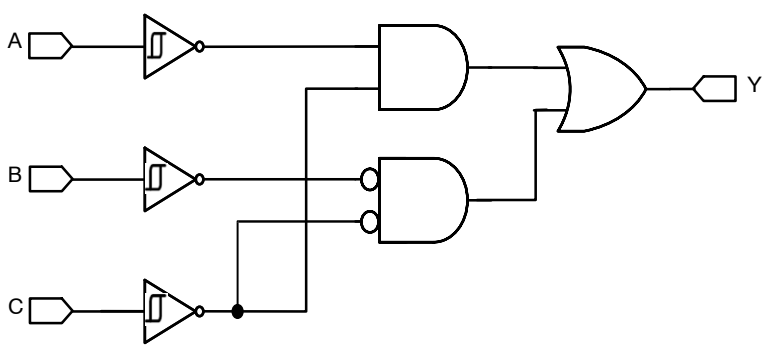
Table 1 provides a list of the functions that are available in the industry standard ‘57’, ‘58’, ‘97’, ‘98’ and ‘99’ configurable gates. Configurable logic ICs are available in a number of different logic technologies that offer a range of operating voltages and performance specifications. Appendix A provides an overview of the attributes of the ON Semiconductor configurable logic devices.

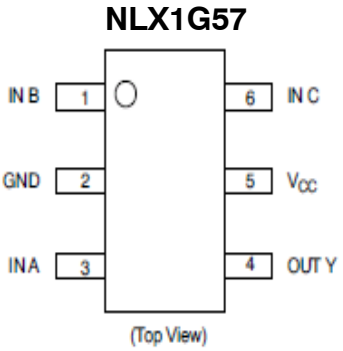
Table 1. SUMMARY OF THE LOGIC FUNCTIONS AVAILABLE WITH THE CONFIGURABLE LOGIC GATES

Part Number / Function NL7SZxx NLX1Gxx	57	58	97	98	99
Buffer	✓	✓	✓	✓	✓
Inverter	✓	✓	✓	✓	✓
2−to−1 MUX / Selector			✓		✓
2−to−1 MUX / Selector (with inverted output)				✓	✓
2−input AND	✓		✓		✓
2−input AND (with 1−inverted input)		✓	✓	✓	✓
2−input NAND		✓		✓	✓
2−input NAND (with 1−inverted input)	✓		✓	✓	✓
2−input OR		✓	✓		✓
2−input OR (with 1−inverted input)	✓		✓	✓	✓
2−input NOR	✓			✓	✓
2−input NOR (with 1−inverted input)		✓	✓	✓	✓
2−input XOR		✓			✓
2−input XOR (with 1−inverted input)					✓
2−input XNOR	✓				✓
Available Logic Configurations	7	7	9	9	15

The desired logic function is determined from the Functional Truth Table provided in the data sheets. For example, Figure 1 shows how to use the ‘57’ as a 2−input AND gate or the equivalent 2−input NOR with inverted inputs. The AND function is selected by setting input pin A to a logic ‘1’ which selects the bottom four rows of the truth table. The B and C pins serve as the inputs while the output is provided by pin Y.

’57’ FUNCTIONAL DIAGRAM

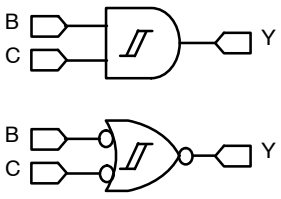




’57’ FUNCTIONAL TABLE

Input			Output
A	B	C	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

Design Example:
2−Input AND / NOR
Input A = H



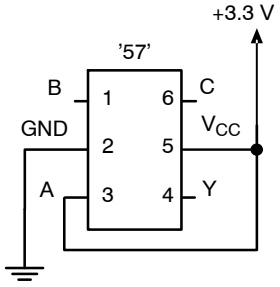


Figure 1. This design example shows how to implement a 2−input AND gate with the NLX1G57 configurable logic gate

The Schmitt trigger inputs are an important feature of the configurable logic gates. Schmitt trigger inputs have two different switching points, as shown in Figure 2. The difference or hysteresis between the Vt+ and Vt− input switching threshold voltages is an important attribute with slow transitioning signals. The Schmitt trigger input pins are an essential feature in the pulse generation and signal conditioning circuits that use an external resistor and capacitor to delay the input signal.

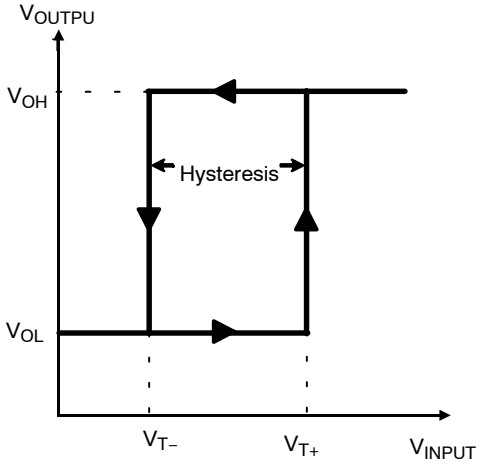


Figure 2. The inputs of the configurable logic gates have Schmitt trigger inputs with hysteresis that prevent glitching on the output signal

Pulse Generation Circuits

Often it is necessary to delay either one or both edges of a clock signal. Figures 3, 4 and 5 provide edge delay circuits that are created by adding an external resistor and capacitor to the input pin of the logic gate. The resistor and capacitors delay the low−to−high and/or high−to−low transition times of the output signal by an amount that is proportional to the RC product. Note that the delay times t_{d1} and t_{d2} of the dual delay circuit will not be equivalent due to the hysteresis of the Schmitt trigger inputs.

Dual Edge Delay

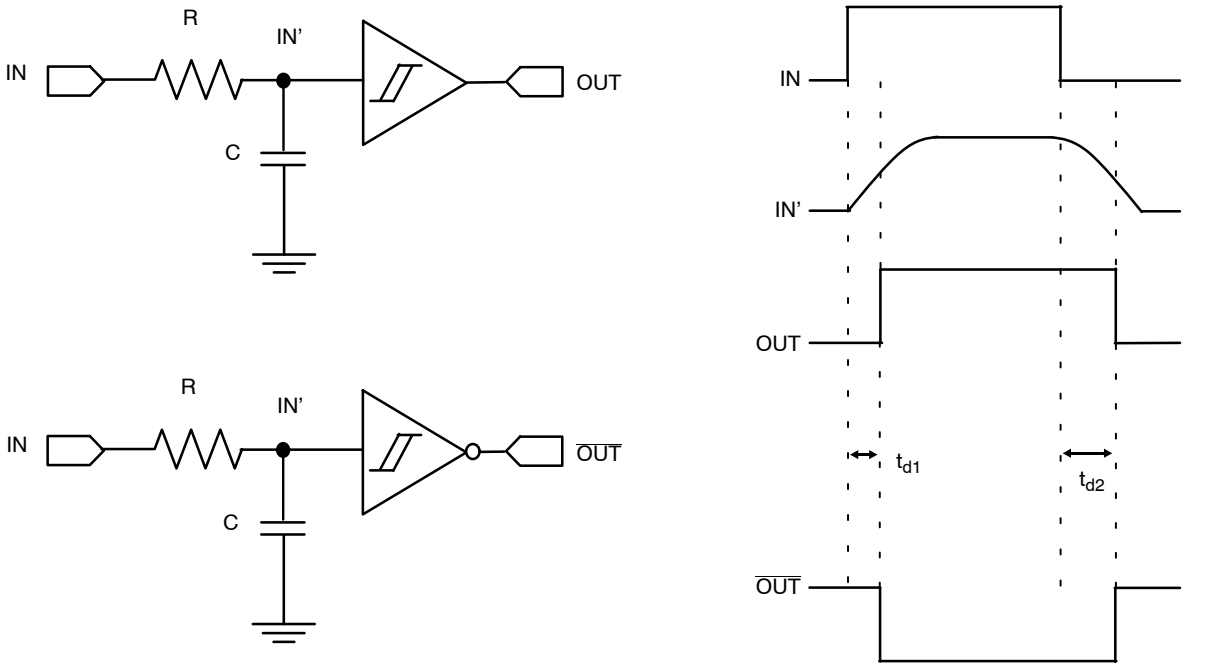


Figure 3. A resistor, capacitor and buffer / inverter delay the leading and rising edges of an input pulse

Leading Edge Delay

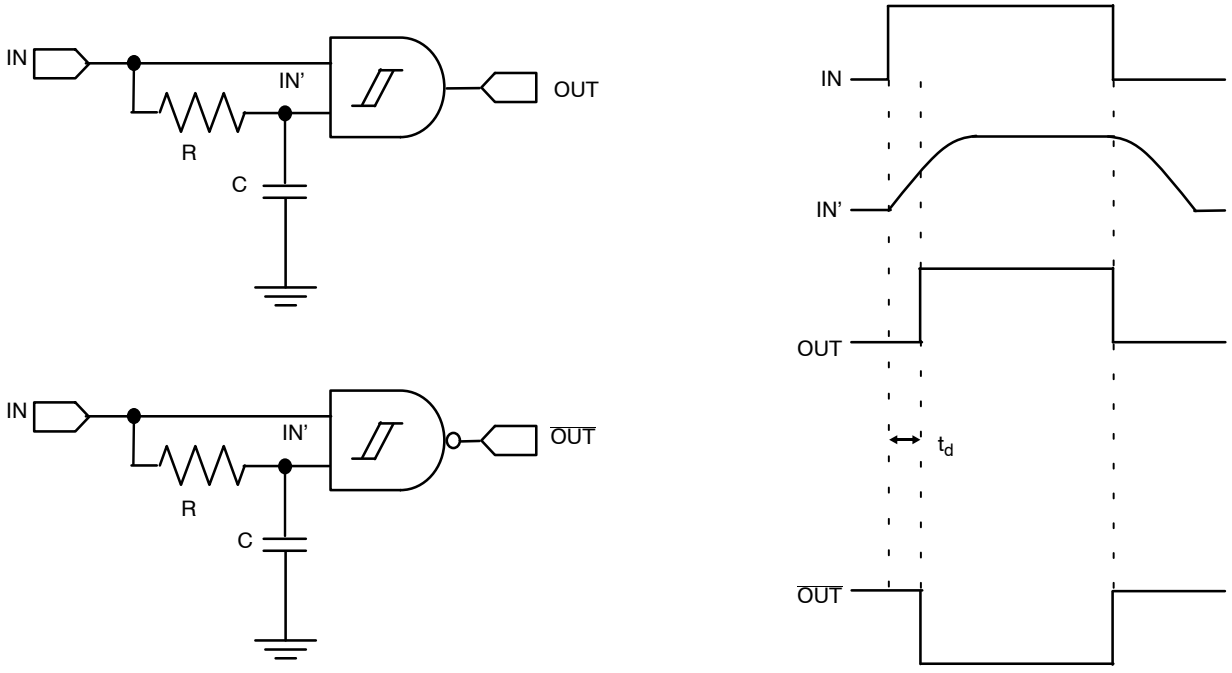


Figure 4. A leading edge delay circuit is created with a resistor, capacitor and an AND / NAND gate

Trailing Edge Delay

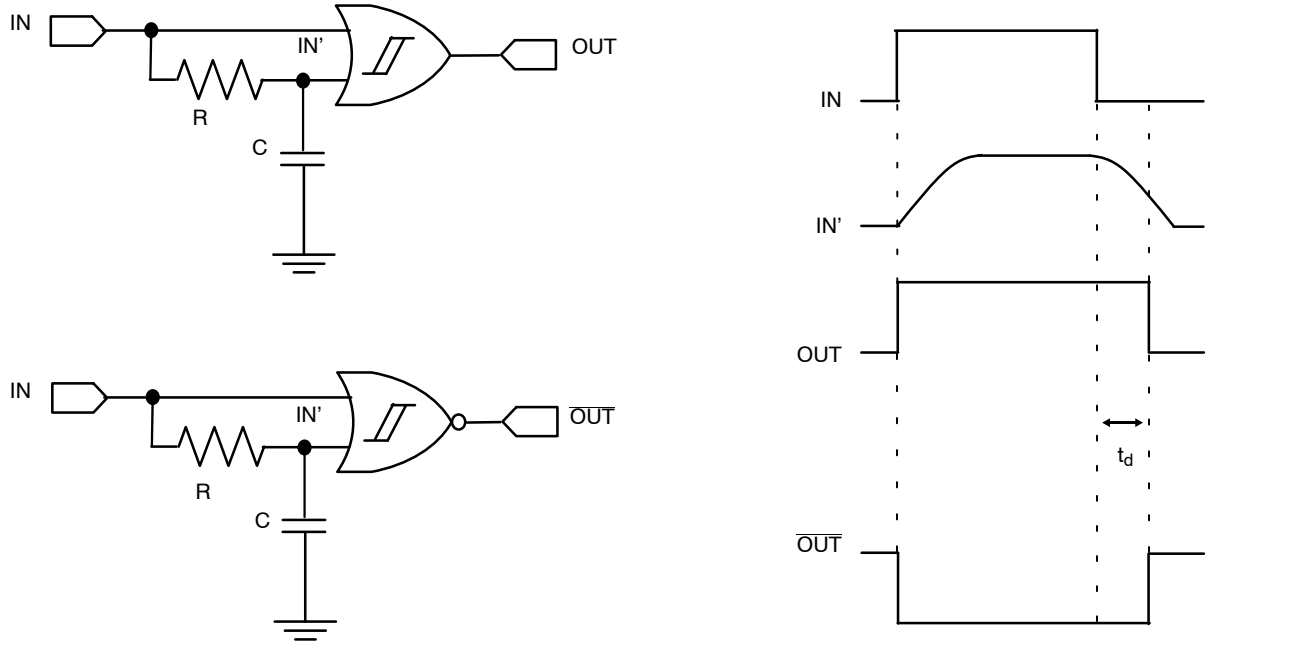


Figure 5. The trailing edge delay circuit is provided with a resistor, capacitor and OR / NOR gate

Edge detectors are a convenient circuit to generate a second timing signal after the detection of the rising or falling edge of a clock signal. An exclusive OR gate provides a dual edge detector circuit, as shown in Figures 6 and 7. In addition, the dual edge detector circuit functions as a frequency doubler because a pulse is created on both the leading and trailing edges of the input signal. The pulse widths of the two pulses (t_{w1}, t_{w2}) are proportional to the value of the resistor and capacitor. In contrast, the leading and trailing edge detection circuits, shown in Figures 8 and 9, use an AND / NAND gate to provide a single detection pulse.

Dual Edge Detector / Frequency Doubler−Option I

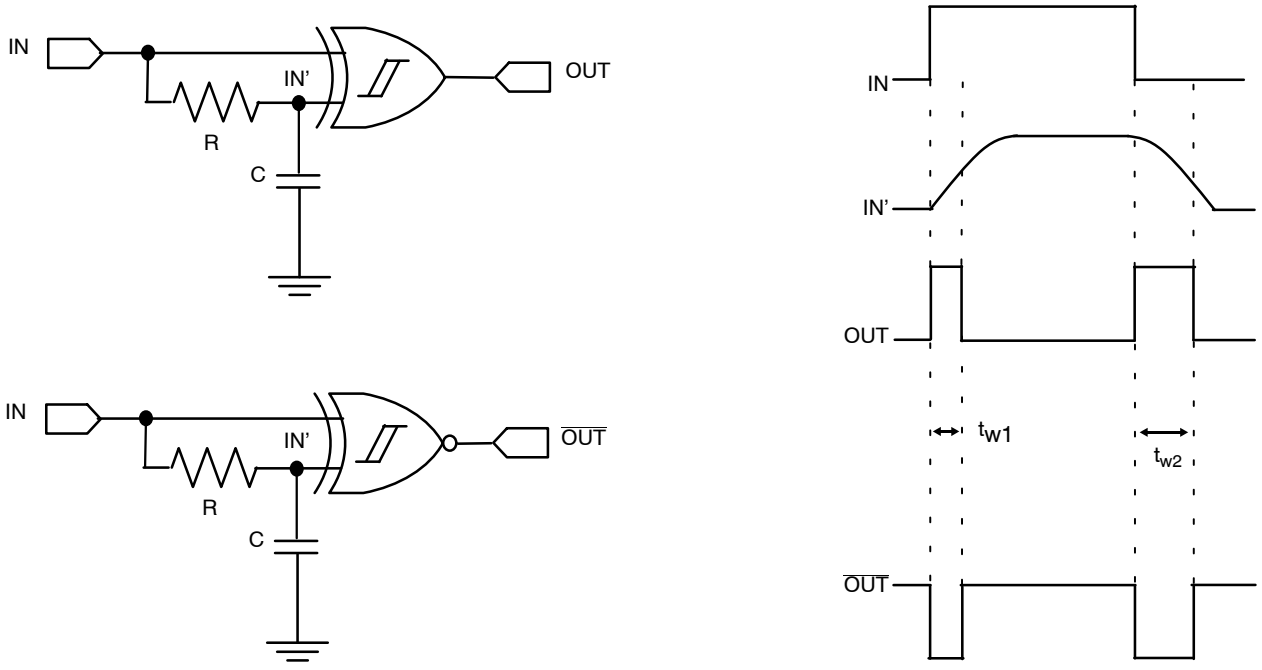


Figure 6. A resistor, capacitor and XOR / XNOR gate provides one option to create a dual edge detector or frequency doubler

Dual Edge Detector / Frequency Doubler−Option II

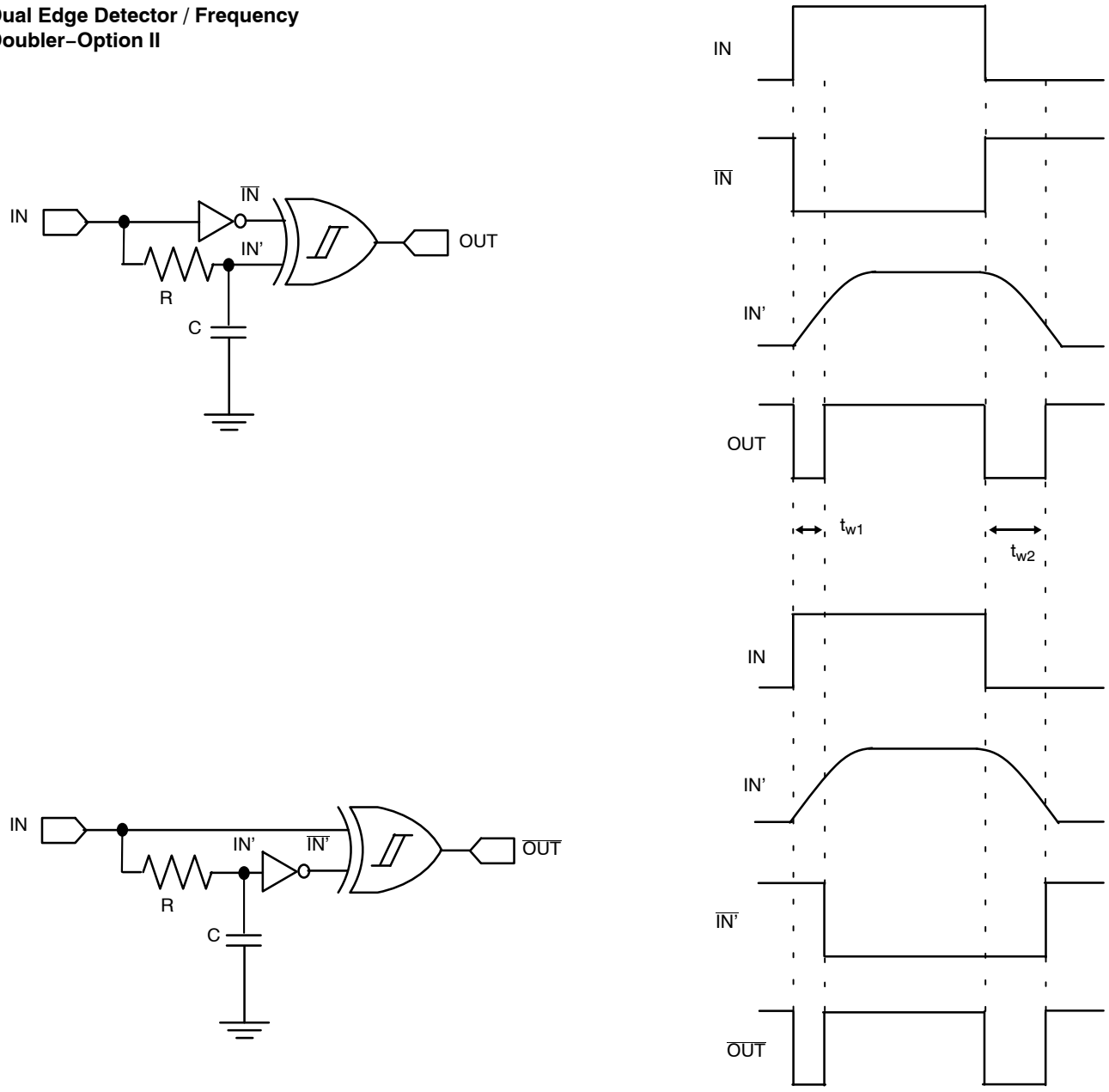


Figure 7. A resistor, capacitor and XOR gate with an inverted input forms an alternative method to create a dual edge detector or frequency doubler

Leading Edge Detector

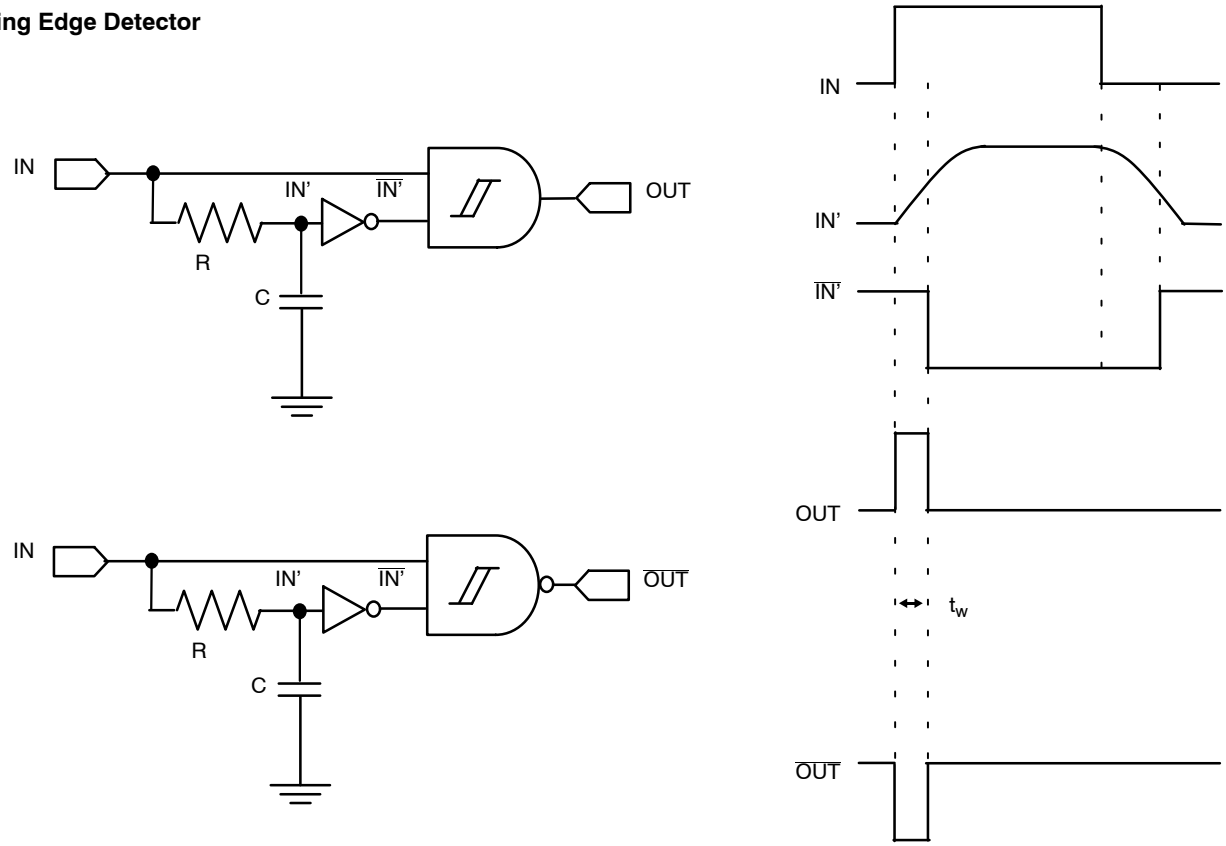


Figure 8. The leading edge detector circuit is provided by a resistor, capacitor and AND / NAND gate with an inverted input

Trailing Edge Detector

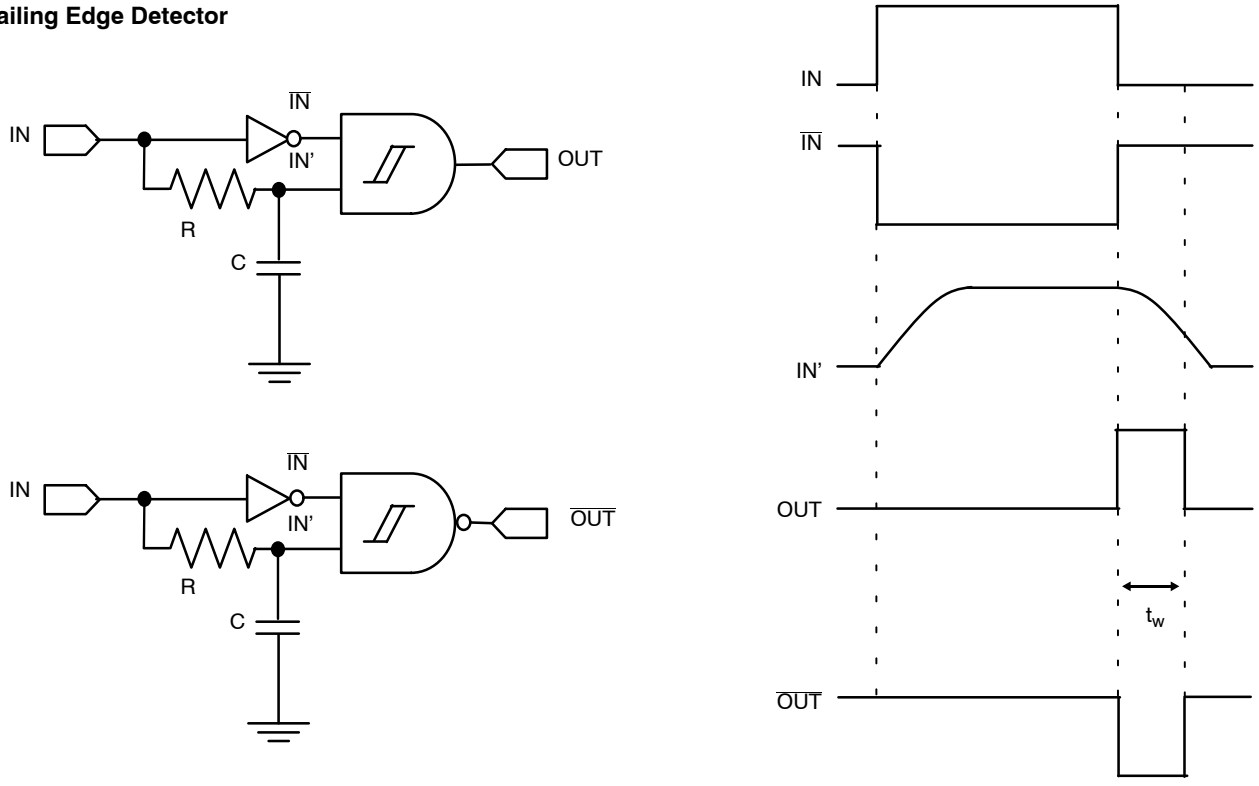


Figure 9. A trailing edge detector is created from a resistor, capacitor and an AND / NAND gate with an inverted input

Signal Conditioning Circuits

Configurable logic ICs can function as a multiplexer or voltage translator. The ‘97’, ‘98’ and ‘99’ devices contain a 2−to−1 selector that is useful in data multiplexing applications, as shown in Figure 10. Another popular application is to use the configurable gate to shift the input and output logic levels, as shown in Figure 11. Note that the overvoltage tolerance feature is not available in all configurable gates; however, it is a standard feature in the ON Semiconductor devices.

2−to−1 Multiplexer / Selector

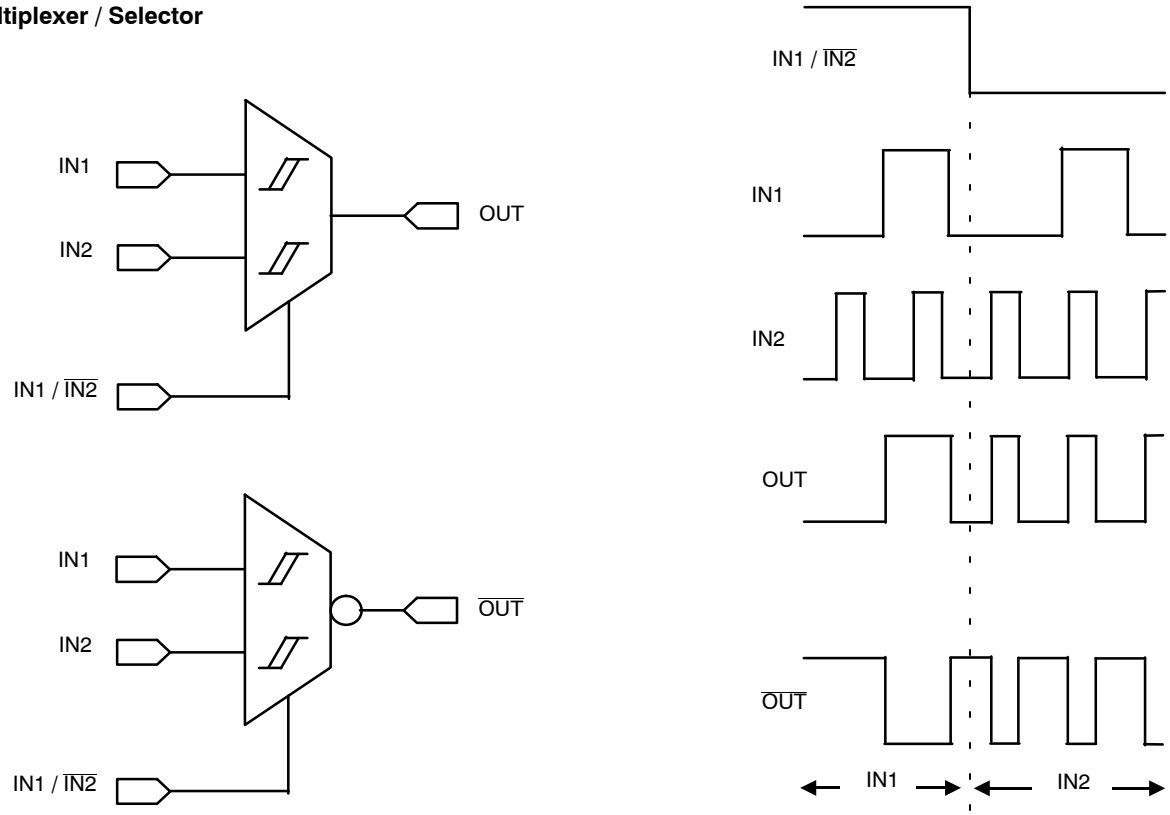


Figure 10. The configurable logic gate can be used as a two−to−one multiplexer / selector

Voltage Translator
(V_{IN} > V_{CC})

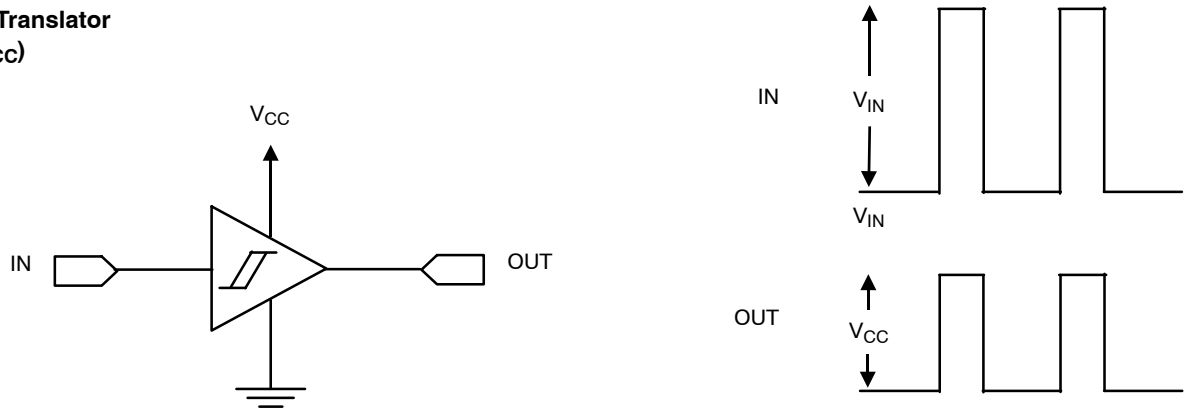


Figure 11. The overvoltage tolerant (OVT) feature on the input pin provides a simple method to create a high−to−low voltage logic translator

The power indicator circuit shown in Figure 12 provides a low cost alternative to analog comparator circuits that monitor the amplitude of a voltage supply. The external resistor and capacitor delay the powerup sequence until the voltage supply has stabilized. In contrast, a diode is used to quickly discharge the capacitor at powerdown and provide a signal that can be used to initiate the shutdown of power sensitive components.

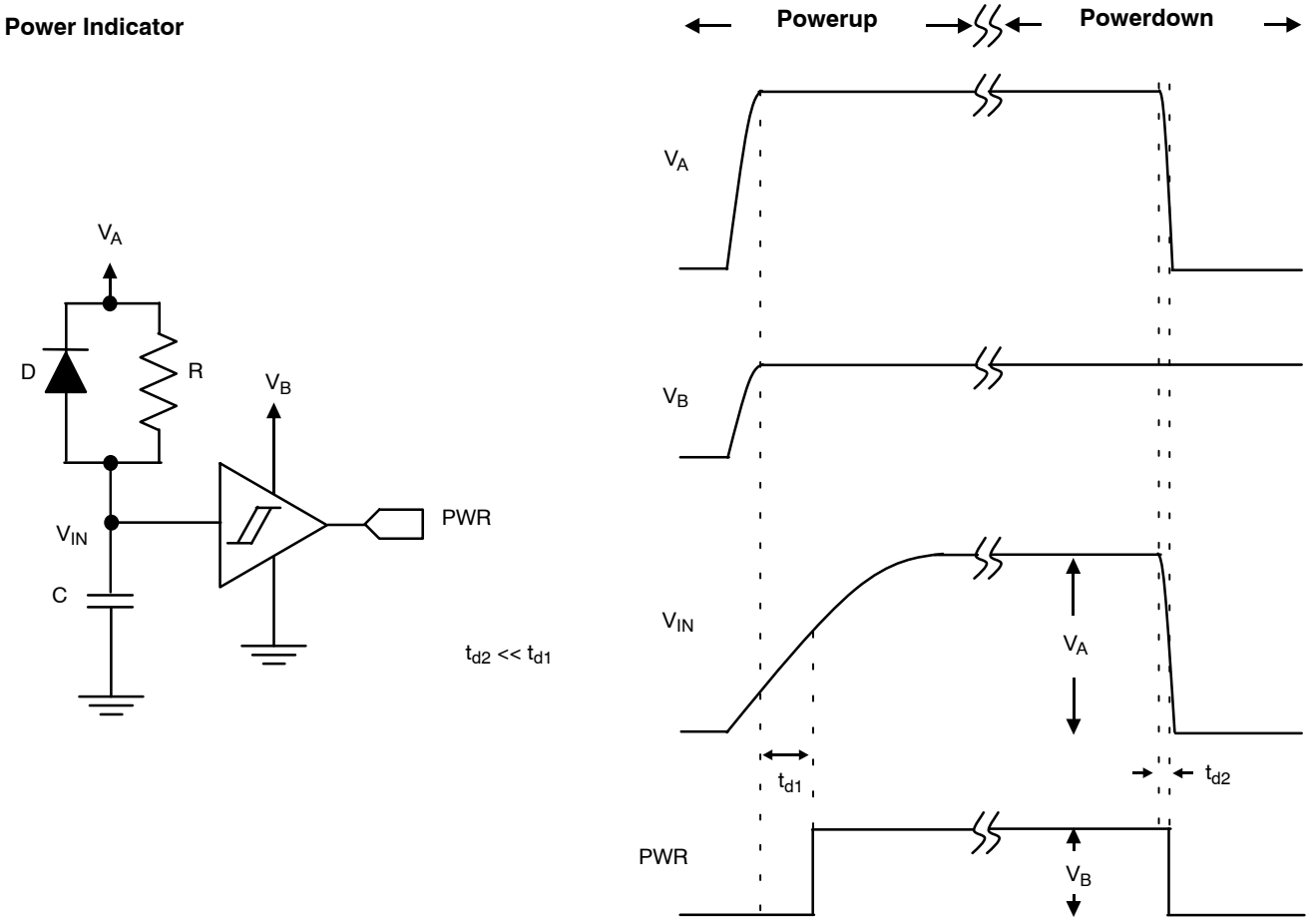


Figure 12. A 'Power Good' indicator can be created from a diode, resistor, capacitor and buffer The circuit provides a delay at powerup and a quick warning at powerdown

Switch debouncing, oscillators and Non−Return−to−Zero (NRZ) to Return−to−Zero (RZ) data converters are additional circuits that can be implemented with a configurable gate. A switch debouncer circuit is shown in Figure 13 that is formed with two resistors, a capacitor and buffer gate. Figure 14 provides an example of a simple oscillator circuit that can be used to create either a clock or gated clock signal. The AND gate can be used to combine a clock signal with a NRZ input signal to create a RZ output signal, as shown in Figure 15.

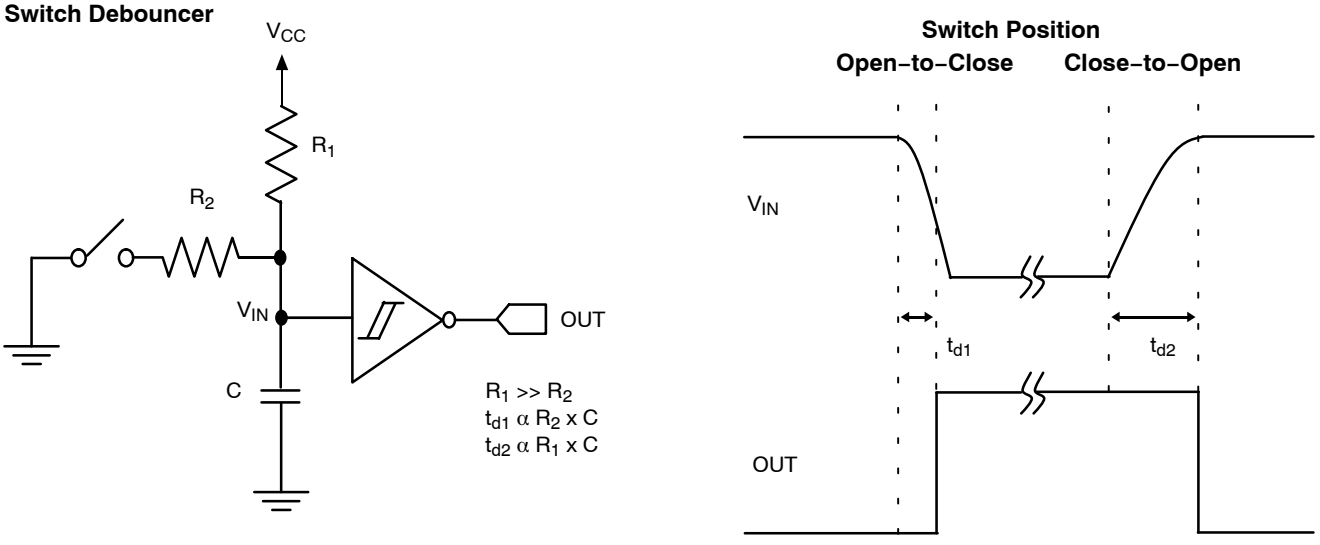


Figure 13. The switch debouncer circuit provides time delays that prevent glitching on the output signal

Oscillators

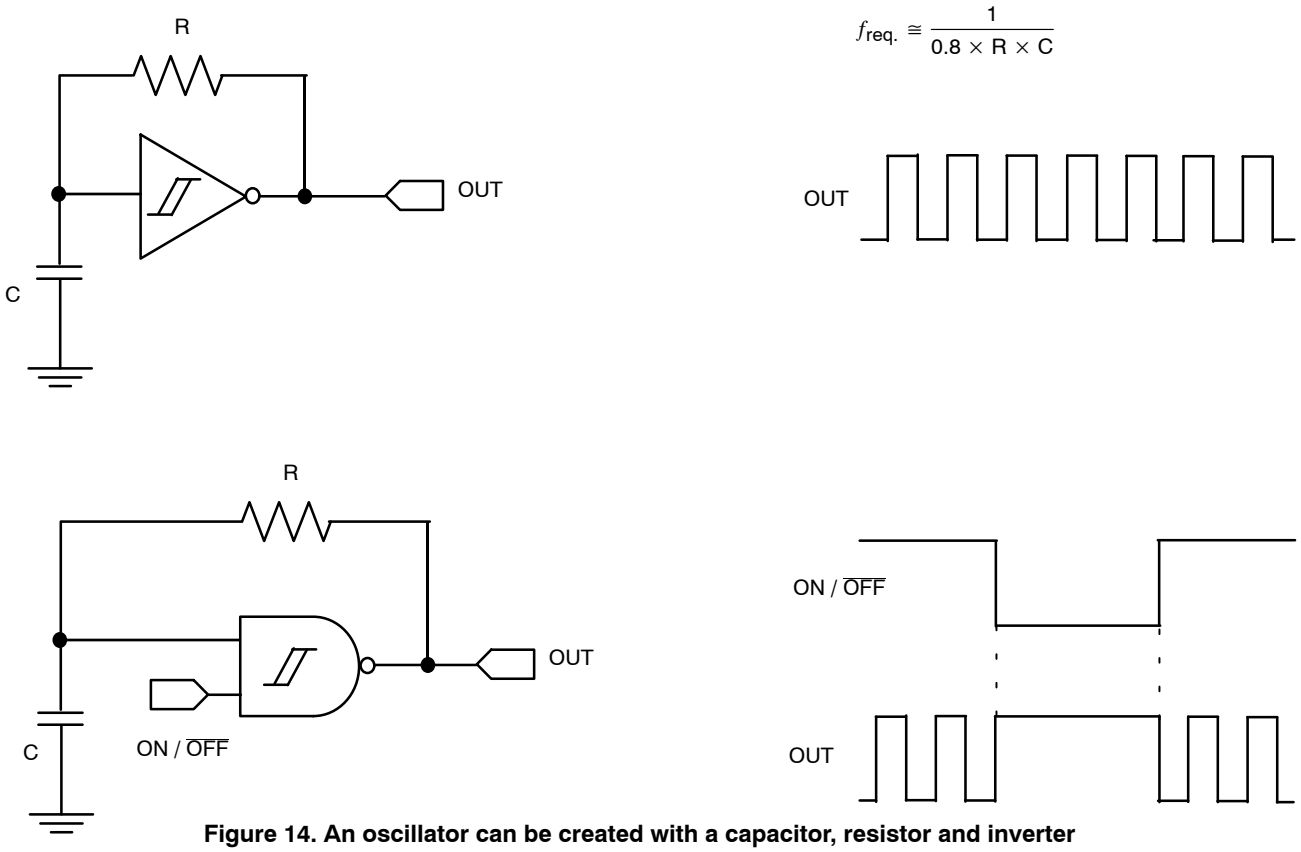


Figure 14. An oscillator can be created with a capacitor, resistor and inverter Substituting a NAND gate for the inverter creates a gated oscillator

NRZ−to−RZ Data Converter

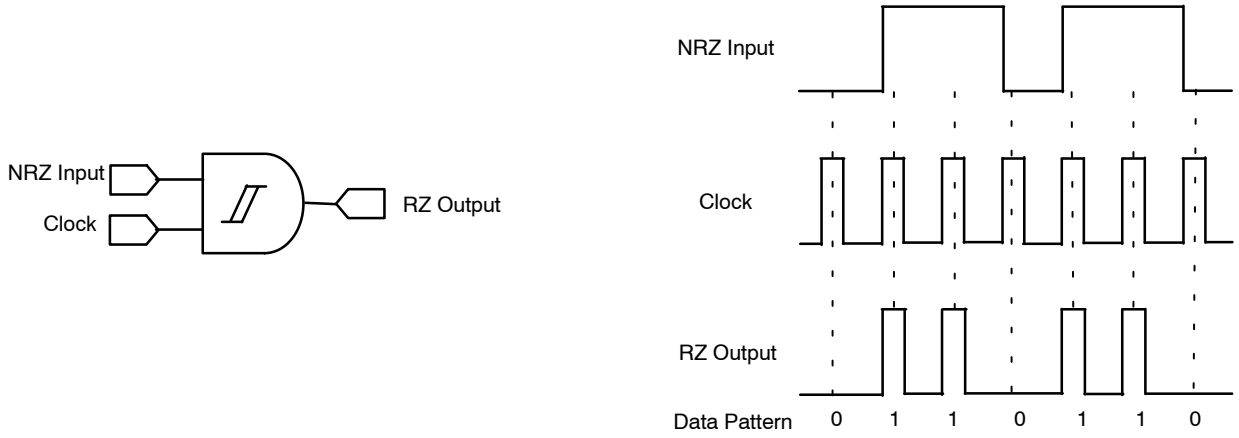
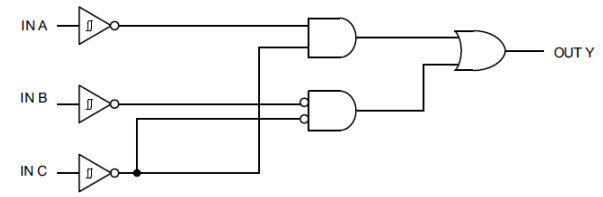
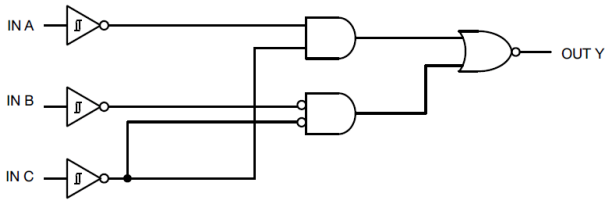
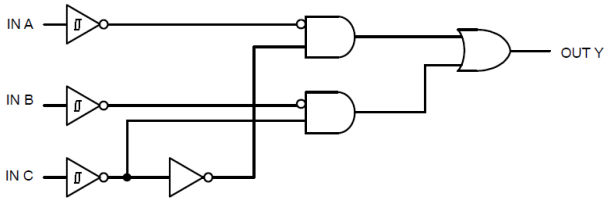
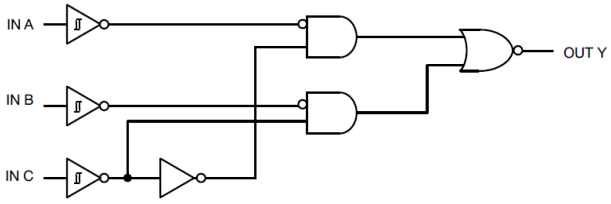
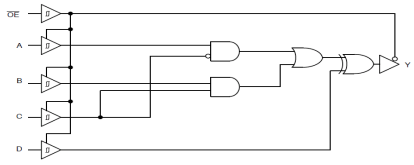


Figure 15. A Non−Return−to−Zero (NRZ) input signal can be converted to a Return−to−Zero (RZ) output with an AND gate

References

1. Chenier, G. “Configurable Logic gates’ Schmitt Inputs Make Versatile Monostables”, *EDN*, May 25, 2006.

APPENDIX A: ON Semiconductor's Configurable Multifunction Logic Gates

Device	P/N#	Features
'57' 	NL7SZ57 NLX1G57	• SC−88 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V • ULLGA6 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V
'58' 	NL7SZ58 NLX1G58	• SC−88 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V • ULLGA6 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V
'97' 	NL7SZ97 NLX1G97	• SC−88 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V • ULLGA6 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V
'98' 	NL7SZ98 NLX1G98	• SC−88 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V • ULLGA6 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V
'99' 	NLX1G99	• ULLGA8 Package • OVT Inputs • V_{CC} = 1.65 to 5.5 V • Output Enable

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